Title: "Low Power Silicon Thermal Sensors and Microfluidic Devices based on the use of Porous Silicon Sealed Air Cavity technology or Microchannel technology"

Field of the invention

This invention relates to low power silicon thermal sensors and microfluidic devices, which use a micromachining technique to fabricate electrochemically porous silicon membranes with a cavity underneath. In the case of thermal sensors the structure used is of the closed type (porous silicon membrane on top of a cavity), while in microfluidics the same technique is used to open microchannels with a porous silicon membrane on top.

Description of the related art

Silicon thermal flow sensors are based on heat exchange between the fluid and the hot parts of the device, which are kept at relatively high temperature, of the order of 100 – 180 °C. In silicon thermal gas sensors, this temperature has, sometimes, to exceed 400 °C. In order to keep the temperature constant, the electric power on the heater has to compensate thermal losses due to conduction, convection and radiation. Losses due to conduction through the substrate on which the active elements of the device are fabricated can be minimized if this substrate is a thin membrane with a cavity underneath, instead of bulk crystalline silicon, (thermal conductivity of bulk silicon: K = 145 W/m.K, thermal conductivity of air: $K = 2.62 \times 10^{-2}$ W/m.K). Different methodologies were developed so far for the fabrication of membranes in the form of bridges, suspended over a cavity in bulk silicon. By using bulk silicon micromachining techniques, A.G. Nassiopoulou and G. Kaltsas [Patent N° OBI 1003010, Patent N° PCT/GR/00040, published by WIPO 12/11/1998] and G. Kaltsas and A. G. Nassiopoulou [Mat. Res. Soc. Symp. Proc. Vol. 459 (1997) 249, Microelectronic Engineering 35 (1997) 397] fabricated suspended polycrystalline or monocrystalline silicon membranes, using only front side optical lithography and porous silicon locally formed on bulk crystalline silicon, which is then removed in order to form a cavity under the membrane. Dusko et al. [Sensors and Actuators A, Vol.60, (1997) 235] , using a similar technique, fabricated suspended silicon nitride membranes. Both of the above techniques were used to fabricate silicon thermal sensors.

A gas flow sensor was fabricated by G. Kaltsas and A. G. Nassiopoulou, Sensors and Actuators A, 76 (1999), p. 133-138 and a gas sensor by C. Ducso, M. Adam, E. Vazsonyi, I. Szabo and I. Barsony, Eurosensors XI, Warsaw, Poland, Sept. 21-24, 1997). However, there is an important drawback in the above techniques. It is related to the fragility of the structures which makes any processing after membrane formation very difficult. An alternative method was proposed and used by A. G. Nassiopoulou and G. Kaltsas (Greek patent No 1003010) and G. Kaltsas and A. G. Nassiopoulou, ["Front-side bulk silicon micromachining using porous silicon technology", Sensors and Actuators: A, 65, (1998) p.175-179]. It uses slightly oxidized porous silicon as a material for local thermal isolation on bulk silicon. This approach offers important advantages related to the mechanical stability of the structure and the compatibility with further silicon processing. It has been successfully used to fabricate silicon thermal gas flow sensors by G. Kaltsas and A. G. Nassiopoulou [Sensors and Actuators 76 (1999) 133, Phys. Stat. Sol. (a) 182 (2000) 307]. In the present patent we propose a methodology to improve the above technique by combining the advantages of using a cavity (better thermal isolation) with the advantages of a rigid structure. The proposed structure is composed of a cavity sealed with porous silicon and fabricated in one process step by electrochemistry. Although electrochemistry has been successfully used to manufacture non-planar free-standing porous silicon structures [G. Lammel, Ph. Renaud, "Free-standing,mobile 3-D porous silicon microstructures", Sensors and Actuators A, 85, (2000) p.356] and buried multi-walled microchannels [R. Willem Tjerkstra, Johannes G. E. Gardeniers, John J. Kelly and Albert van den Berg. "Multi-Walled Microchannels: Free-Standing Porous Silicon Membranes for Use in μTAS", Journal of MicroElectroMechanical Systems, vol. 9 ,No 4 ,(2000) p.495] that can be applied in the area of actuators and μTAS respectively, the specific technology is the only one which provides close-type structures composed of a planar porous silicon membrane, on top of a cavity on bulk crystalline silicon. The porous silicon membrane is perfectly aligned with the crystalline silicon surface and the cavity lies underneath. The technology can be used to provide a localised thermally isolated region for the creation of a low power silicon thermal sensor or an open microchannel with a porous silicon membrane on top for the creation of a microfluidic device. The provided thermal isolation is better than in the case of porous silicon thick films without cavity underneath.

Summary of the invention

It is an object of this invention to provide a method for the fabrication of silicon thermal sensors with improved thermal isolation, based on the use of a sealed cavity on which the active elements of the sensor are developed. The sealed cavity is fabricated on bulk silicon by a two-step electrochemical process in which in the first step porous silicon is formed locally on bulk silicon by electrochemical dissolution with an anodization current below the limit for electropolishing and in a second step the current is increased so as the process is turned to electropolishing for the fabrication of a cavity underneath the porous layer. The silicon thermal sensor devices based on the above structure combine the good isolation properties offered by suspended membranes with the advantage of having a rigid structure. In the Greek patent N° OBI 1003010, a rigid and mechanically stable structure was also proposed, based on porous silicon locally formed on bulk silicon in order to provide local thermal isolation. The present approach is an improvement of that structure, because it offers both mechanical stability by the planar structure and better thermal isolation by the cavity underneath the porous layer. The critical value of current density for electropolishing (Jps) depends on the electrochemical solution used and on the resistivity and type of the silicon substrate. The thickness of the porous layer and the depth of the cavity are adjusted by adjusting the current density and the anodization time for the specific solution used. The smoothness of the bottom surface and sidewalls of the cavity depend also on the electrochemical solution used. A schematic presentation of the above described structure is shown in fig.1, where (1) is the silicon substrate, and (2) is the porous silicon layer on top of the cavity (3).

It is also an object of the present invention to provide a thermal flow sensor based on the above method. This sensor is illustrated in fig. 2. It is composed of a silicon substrate (1) on which a closed structure of a porous silicon membrane (2) with a cavity underneath (3) is formed locally by an electrochemical dissolution of silicon in an HF:ethanol solution after the appropriate deposition and patterning of a masking layer. Depending on the thickness of the porous layer and the depth of the cavity, the mask for porous silicon formation is either a resist layer, or silicon nitride or a bilayer of SiO_2 and polycrystalline silicon. An ohmic contact (13) has been created on the back side of the silicon substrate prior to the electrochemical process. The active elements of the sensor are composed of a heater (4) and two thermopiles (6,7) on each side of the heater. The number of thermocouples in each thermopile depends on the needed sensitivity of the device. The hot contacts of the thermocouples (5) are on porous silicon and the cold

contacts (10) on the bulk crystalline silicon substrate (1). The required interconnections (11) and metal pads (12) are formed by aluminum deposition and patterning. A passivation layer may be also deposited on top of the thermal flow sensor, consisted of an insulating layer, for example silicon oxide, or silicon nitride or polyimide. An electrical isolation layer (14) is deposited on top of the silicon substrate (1) so as to assure the electrical isolation between the sensor elements and the substrate. The thermocouple material is n-type poly/Al or n-type/p-type poly. The first case limits the temperature of operation of the device at around 400 °C, while the second permits operation at temperatures up to ~ 900 °C. The heater is composed of p-type polycrystalline silicon and it is maintained at constant power or constant temperature by using an external electronic circuit, which stabilizes the power or the temperature by providing a current feedback if the temperature changes. The device can also operate at constant current on the heater, but the use of constant power is better in the case of a high flow range. Indeed, under flow the resistor is instantly cooled down by the gas flow and this causes a slight change of its resistance, which gives a measurable effect to the thermopiles output at high flow. This effect is minimized if the resistance change is compensated by a slight change in the current, so as to keep the power consumption or the temperature on the heater constant.

It is also the object of the present patent to propose the use of the heated resistor both as heater and as temperature sensing element. Alternatively, two resistors may be integrated on both sides of the heater for temperature sensing. In the above two cases the power supply and readout electronics are different than in the case of the two thermopiles on each side of the heater.

The thermal isolation by porous silicon with a cavity underneath, compared to the use of a single porous silicon layer in contact with the substrate offers the advantage of reducing power consumption and increasing the sensitivity of the device. Simulations carried out using MEMCAD V.4.8 package by MICROPROSM showed that the improvement depends on porous layer thickness and air cavity depth. Fig. 3 shows the effect of porous layer thickness on the temperature of the heater for a cavity of 20 μm and a heat flux of 8.57×10^6 W/m^2 applied on a 530 μm long polysilicon heater of width 20 μm and thickness 0.5 μm. This corresponds to a supplied power of 71 mW. For comparison, the results of a compact structure, where there is no cavity but instead a 40 μm thick porous layer is added, are shown with a star in the same figure. Fig. 4 shows the temperature on the heater for a 5 μm thick porous membrane and a cavity of variable thickness underneath. A comparison between isolation by a 40 μm

compact porous silicon structure and a structure with 20 μm porous silicon membrane on 20 μm cavity is shown in fig. 5. The heater is located at the middle of the membrane.

It is also the object of the present patent to provide a technique based on the use of the porous silicon/cavity technology for the formation of a microchannel under the active elements of the device, which may be used as a flow channel, open on its two endpoints. Such a device is shown in fig.6. It is consisted of a silicon substrate (15) on which a microfluidic channel (16) sealed with a porous silicon layer (17), is formed. The said microfluidic channel has two openings, which serve as inlet (18) and outlet (19) of a fluid. A thin silicon dioxide layer (25) is deposited on top of the channel for electrical isolation. The active elements of the thermal flow device are composed of a polysilicon heater (20) and two polysilicon resistors (21, 22) on each side of the heater. The device is used to measure the micro-flow developed into the microchannel. The heater is kept at a certain temperature and the flow measurement is based on sensing the temperature difference induced by the fluid between the two polysilicon resistors (21, 22) lying on the left and right side of the heater (20) in the upstream and downstream of the flow. The heater and resistors are connected to aluminum pads (23) through aluminum interconnects (24). A passivation layer can be deposited on top of the sensor, consisted of silicon oxide or silicon nitride or polyimide. The main advantage of this technology is that microflows can be formed and measured. This technology also offers important advantages in the case of liquid flows, since the liquid will not be in contact with the active elements of the device and so there is no need for complicated passivation schemes. It also offers advantages in gas flow measurements if the gas is corrosive.

It is also the object of the present patent to provide a thermal sensor device for gas sensing based on the use of porous silicon/cavity technology for local thermal isolation on silicon.

It is also the object of the present patent to provide a silicon thermal sensor for detection of infrared radiation, based on the use of porous silicon/cavity technology for local thermal isolation on silicon.

It is also the object of the present patent to provide a silicon thermal device for thermoelectric power generation, based on the use of porous silicon/cavity technology for local thermal isolation on silicon.

It is also the object of the present patent to provide a silicon thermal device for humidity sensing, based on the use of porous silicon/cavity technology for local thermal isolation on silicon.

Brief description of drawings

Fig. 1 is a schematic representation of the porous silicon layer over a cavity in bulk crystalline silicon.

Fig. 2 shows a schematic view of a thermal sensor using porous silicon/cavity technology.

Fig. 3 shows the temperature on heater for thermal isolation by porous silicon of variable thickness over a cavity.

Fig. 4 shows the temperature on heater for thermal isolation by a cavity of variable depth underneath a porous silicon layer.

Fig. 5 shows the temperature distribution around the heater for thermal isolation by porous silicon and by porous silicon over a cavity.

Fig.6 is a schematic view of the flow sensor with a microchannel underneath.

Description of the preferred embodiments

Fig.1 is a schematic representation of a silicon substrate (1) with a porous silicon layer (2) on top of a cavity (3). The whole structure is used for local thermal isolation on bulk silicon.

Fig.2 is a schematic representation of a silicon thermal gas flow sensor. The base material is p-type silicon (1) in which a porous silicon membrane (2) with a cavity (3) underneath is formed.

On top of the porous silicon cavity area a polysilicon resistor (4) is formed and two series of thermocouples are integrated on each side of this resistor (6, 7). The hot contacts (5) of these thermopiles lie on porous silicon and the cold contacts (10) on bulk crystalline silicon. There are also aluminum pads (12) used as electrical contacts.

Fig. 3 shows the temperature on heater for thermal isolation by porous silicon of variable thickness over a cavity for a power of 8.57×10^6 W/m^2 applied on the heater.

Fig. 4 shows the temperature on heater for thermal isolation by a cavity of variable depth underneath a porous silicon layer.

Fig. 5 shows the temperature distribution around the heater for thermal isolation by 40 μm thick porous silicon film and by 20 μm thick porous silicon membrane over a 20 μm cavity.

Fig. 6 shows a microfluidic flow sensor based on the use of porous silicon/cavity technology. In (a) the top view and in (b) a cross sectional representation is shown, where (15) is the silicon substrate, (17) the porous silicon layer, (16) the microfluidic channel, (18, 19) the inlet and outlet of

the microfluidic channel, (20) is a polycrystalline silicon resistor used as heater, (21, 22) are polycrystalline silicon resistors used as temperature sensing elements, (24) are aluminum interconnects and (23) are aluminum contact pads.